DESCRIPTION

SWITCHED-CURRENT ANALOGUE-TO-DIGITAL CONVERTER

This application is a 371 of PCT/IB03/03027 Filed on 7/08/2003.

The invention relates to a switched-current pipeline analogue-to-digital converter and an electronic device comprising such a converter.

The general architecture of a typical N-bit switched-current pipeline analogue-to-digital converter (ADC) is illustrated in Figure 1. It comprises an analogue current input 10 and N cascaded conversion stages $S_1...S_N$. Each stage generates one bit $b_1...b_N$ and, except for the last stage, an analogue residue current $r_1...r_{N-1}$ which is passed to the following stages for conversion. De-skew logic 20 re-times the bits and provides bits $B_1...B_N$ simultaneously. The general architecture of each conversion stage S_i, except the last S_N, is illustrated in Figure 2 and comprises a sample-and-hold (S/H) circuit 30 for sampling the input current r_{i-1}, a current comparator 40 for generating one bit b_i by comparing the input current r_{i-1} with a reference threshold current, a current digital-to-analogue converter (DAC) 50 for converting the bit b_i to a current, and a summing means 60 for generating the residue current r_i as the difference between the input current r_{i-1}, as delivered via the current memory 30, and the current delivered by the DAC 50, I_{DAC}. The last conversion stage S_N has only a current comparator 40, for providing b_N, as no residue is required.

A fast conversion speed is required in electronic devices that process signals having a wide bandwidth. An example of such an electronic device is a wireless receiver in which a received signal is digitised before demodulation in a digital signal processor. Another example of such an electronic device is a digital recorder that incorporates an ADC for converting an analogue signal to a digital signal prior to writing the digital signal to a recording medium. In order to achieve a fast conversion speed in an ADC it is desirable to use an